REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated November 1, 2006. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 5-10, 14 and 16-19 are under consideration in this application. Claims 1-4 and 11-13 and 15 are being cancelled without prejudice or disclaimer. Claims 5-6, 8-10 and 14 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 18-19 are being added.

All the amendments to the claims and the specification are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Allowable Subject Matter

Claims 16-17 were allowed, and claim 3 would be allowed if rewritten in independent form including all limitations of the base claim and any intervening claims.

Prior Art Rejection

Claims 1-2, 4-12 and 14-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants admitted prior art depicted in Fig. 14 ("AAPA". pp. 3-5) in view of US Pub. No. 2002/0167897 of Tateno et al. (hereinafter "Tateno"). This rejection has been carefully considered, but is most respectfully traversed in view of the claims currently on file, as more fully discussed below.

The signal communication apparatus 102 of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals. The apparatus 102 of the invention (for example, the 1st embodiment depicted in Figs. 1-2; pp. 13-17), as now recite din claim 14, comprises a data signal reception section 118 for receiving data signals Txd1, Txd2, Txd3, ... Txdn that have been transmitted, and the data signal reception section 118 comprises: a number *a* of ***clock signal extraction circuits***, each of which

extracting a clock signal from each of *a*-bit data signals in ***n-bit parallel data signals*** Txd1, Txd2, Txd3, ... Txdn that have been received, where *a* is an integer such that $2 \leq a < n$ (p. 7, last paragraph); a clock signal selection circuit 111 for selecting a single clock signal (b=1 in Claim 16) from the extracted *a* clock signals SCK1-SCKa, the single clock signal being designated as a reference clock signal SCK; a number *n* of phase adjusting circuits 1081, 1082, 1083, ... 108n for adjusting the phase of the selected reference clock signal ***to produce reproduction clock signals*** RCK1, RCK2, RCK3, ... RCKn for the received n-bit parallel data signals, each reproduction clock signal RCK providing a timing of redigitization of each of the received *n*-bit parallel data signals Txd1, Txd2, Txd3, ... Txdn; and sampling means 1091, 1092, 1093, ... 109n for redigitizing each of received n-bit parallel data signals Txd1, Txd2, Txd3, ... Txdn in accordance with the timing provided by the reproduction clock signal RCK for each bit (last paragraph of cancelled claim 1; "*a reproduction clock signal for each of the n-bits providing the timing for sampling and redigitizing the data signals*" p. 7, lines 7-9; p. 16, line 26). Thus, communication can be resumed as far as data signals other than the data signal Txd1 with an abnormality, that is the n-1 bit data signals, are concerned.

The invention of claim 19 is directed to a signal communication apparatus (for example, the 2nd embodiment depicted in Figs. 3-4; pp. 17-21), wherein the clock signal extraction/selection circuit (p. 18, last paragraph) comprises: a voltage controlled oscillator 314; a number *a* of phase comparators 3131 (Fig. 15) respectively comparing the phase of each of the *a*-bit data signals with that of output signal of each of said voltage controlled oscillators 314; a selector 312 for selecting one output from comparison outputs of said phase comparators 3131; and a loop filter 314 for connecting the selected comparison output to said voltage controlled oscillator 314.

The invention carries out n-bit parallel clock signal transmission, and then re-digitizes the reception signal of each bit that has been attenuated through the transmission line. In particular, a clock signal is extracted from each of a plurality of bits in an n-bit parallel clock signal, only one of the multiple clock signals is selected as a common reference clock signal SCK, and the reference clock signal SCK is adjusted for phase so as to obtain a timing for redigitizing each bit of the n-bit parallel clock signal.

As shown in Fig. 2, during period P1, clock signal SCK1 extracted from data signal Txd1 is used as the reference clock signal SCK. If abnormality arose in the data signal Txd1 at time T1, the rise and fall edges of the data signals cannot be detected due to the abnormality in the data signal Txd1, so that the clock signal SCK1 gradually deviates from

the one-half frequency of the data signal TD/2. Similarly, the frequency of the reproduction clock signal RCK1, RCK2, RCK3, ... RCKn for each bit deviates from the one-half frequency of the data frequency TD/2. As a result, the flip-flop circuits 1091, 1092, 1093, ... 109n cannot correctly redigitize the data signals. If the abnormality in the reference clock signal SCK is detected during period P2. Thus, in period P3, the normal clock signal SCK2 extracted from the data signal Txdn is used as the reference clock signal SCK, so that the generation of the reproduction clock signals RCK2, RCK3, ... RCKn can be resumed (p. 16, last paragraph).

Applicants respectfully submit that none of the cited references teaches or suggests such a "clock signal selection circuit 111 for selecting a single clock signal from the extracted *a* clock signals SCK1-SCKa (in *n-bit parallel data signals*) to be designated as a reference clock signal SCK for producing reproduction clock signals thereby providing a timing of redigitization of each of the received *n*-bit parallel data signals" according to the present invention.

As admitted by the Examiner (p. 4, lines 3-7 of the outstanding Office Action), AAPA fails to disclose redundant clock reproduction circuits and a clock reproduction selector for selecting a number *b* of bits from a number *a* of bits in *n*-bit data signals that have been received, where *a* is an integer such that $2 \leq a < n$, and *b* is such an integer that $1 \leq b \leq a$.

The Examiner asserted (p. 4, lines 7-9 of the outstanding Office Action) that clock extraction redundancy is "well known in the art." However, the Examiner's reliance upon the "common knowledge and common sense" of one skilled in the art for the allegedly "well-known" teachings did not fulfill the agency's obligation to cite references to support its conclusions. Instead, the Examiner must provide the specific teaching of allegations of "well-known" teachings or combination on the record to allow accountability.

> *To establish a prima facie case of obviousness, the Board must, inter alia, show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." Kotzab, 217 F.3d at 1370, 55 USPQ2d at 1317. .... Recently, in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), we held that the Board's reliance on "common knowledge and common sense" did not fulfill the agency's obligation to cite references to support its conclusions. Id. at 1344, 61 USPQ2d at 1434. Instead, the Board must document its reasoning on the record to allow accountability. Id. at 1345, 61 USPQ2d at 1435.*

See In re Thrift, 298 F.3d 1357.

Although the invention applies the general mechanism of redundancy, the invention applies the redundancy on n-bit parallel clock signal transmission to achieve unexpected results or properties. For example, resuming communication as far as clock data signals other than the clock data signal Txd1 with an abnormality (p. 17, lines 6-8). The presence of these unexpected properties is evidence of nonobviousness. MPEP§716.02(a). The unexpected properties were unknown and non-inherent functions in view of the prior art, since the prior art does not inherently achieve the same results.

Tateno's selector 3-12 (Fig. 5: redundant changeover [0085]) was relied upon by the Examiner to provide the teaching of the clock reproduction selector of the preset invention. However, Tateno's redundant transmission-line changeover apparatus is adapted to SONED/SDH devices ([0004]) such that each of nodes connected via duplicated WDM optical ring networks determines whether frame synchronization should be obtained from either a working line W system or a protection line P system (Fig. 15; [0075]). Upon detection of a failure at a location in either of the systems, manually, the selection is switched so as to secure a transmission line ([0009]). Such a changeover is also performed by Tateno's selector 3-12 in Fig. 5, to which the Examiner referred. As such, Tateno only selects either the working line system or the protection line system to independently carry out communications and realize frame synchronization. On the other hand, the present invention extracts clocks redundantly from a plurality of bits in a signal transmission in which a single link of communication is expanded into parallel n-bits, and then one of the extracted clocks is selected. Thus, the present invention and Tateno are essentially different from each other. While Tateno utilizes the selected clock for frame synchronization, the present invention utilizes the selected clock to obtain sampling timing thereby redigitizing each bit of the reception signal.

In addition, the Examiner fails to establish a prima facie case of obviousness by properly bridging the proposed modification of the references necessary to arrive at the claimed subject matter. MPEP§706.02(j). There are numerous ways to combine Tateno's working/protection line selector 3-12 into AAPA, rather than specifically to "select a single clock signal from the extracted *a* clock signals to be designated as a reference clock signal," or more specifically, to "select a single clock signal from the extracted *a* clock signals SCK1-SCKa (in ***n-bit parallel data signals***) to be designated as a reference clock signal SCK for producing reproduction clock signals thereby providing a timing of redigitization of each of

the received *n*-bit parallel data signals" as in the preset invention. The most intuitive combination would be to simply merge Tateno's changeover apparatus with AAPA as they are, rather than selecting bits and pieces from each reference, and then combining those bits and pieces using knowledge or hindsight gleaned from the disclosure of the present invention as a guide to support the combination. The well established rule of law is that each prior art reference must be evaluated as an entirety, and that all of the prior art must be considered as a whole," *Panduit Corp. v. Dennison Mfg. Co.*, 227 USPQ 337, 344 (Fed. Cir. 1985). See *Para-Ordinance Mfg, Inc. v. SGS Importers Intl.*, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995) ("Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor.").

In addition, one skilled in the art will not look into Tateno's selector 3-12 selecting between a working line system and a protection line system to improve AAPA's n-bit parallel clock signal transmission system, since AAPA does not concern reducing frame synchronization loss in frequency and phase in the SONET/SDH ring network ([0026]), which was the alleged motivation the combine (p. 4, lines 16-18 of the outstanding Office Action) as asserted by the Examiner. The alleged reason does not motivate one skilled in the art to combine the teachings as suggested by the Examiner. Applicants respectfully contend that the alleged motivation to combine is improper.

Even if, arguendo, one skilled in the art were motivated to combine the teachings in AAPA and Tateno as suggested by the Examiner, such combined teachings would still fall short in fully meeting the Applicants' claimed invention as set forth in claims 14 and 19 since, as discussed, there is no teaching of "selecting a single clock signal from the extracted *a* clock signals to be designated as a reference clock signal," or particularly "selecting a single clock signal from the extracted *a* clock signals SCK1-SCKa (in ***n-bit parallel data signals***) to be designated as a reference clock signal SCK for producing reproduction clock signals thereby providing a timing of redigitization of each of the received *n*-bit parallel data signals" in either AAPA or Tateno. AAPA does not have any clock signal selector, and Tateno's selector 3-12 only selects between a working line system and a protection line system.

Applicants contend that cited prior art references or their combinations fail to teach or suggest each and every feature of the present invention as recited in independent claims 14 and 19. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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